Localizing faults in Simulink models using STL

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Abstract

Fault-localization is considered to be a very tedious and time-consuming activity in the design of complex Cyber-Physical Systems (CPS). This laborious task essentially requires expert knowledge of the system in order to discover the cause of the fault. A new procedure that aids designers in debugging Simulink hybrid system models, guided by Signal Temporal Logic (STL) specifications shall be presented in this talk. The proposed approach relies on three main components: (1) a monitoring and a trace diagnostics procedure that checks whether a tested behavior satisfies or violates an STL specification, localizes time segments and interfaces variables contributing to the property violations; (2) a slicing procedure that maps these observable behavior segments to the internal states and transitions of the Simulink model; and (3) a spectrum based fault-localization method that combines the previous analysis from multiple tests to identify the internal states and/or transitions that are the most likely to explain the fault.

Biography

Niveditha Manjunath is a PhD candidate at AIT Austrian Institute of Technology and is affiliated to the Vienna University of Technology. She holds a master’s degree from Chemnitz University of Technology, Germany. Her research interests are in fault-oriented V&V methods for CPS from concept to component design, and in particular in system diagnostics and fault localization. She is extending AMT monitoring tool with the system diagnostics capabilities.

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