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Invited Talk hosted by Carole-Jean Wu

"Predicting Timing Violations: A circuit-architectural perspective on robust system design"

FEATURING

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Monday, October 6, 2014 - 10:30 AM – 12:00 PM
BYENG 420

Abstract:

Current and future technology nodes are increasingly susceptible to timing violations, an artifact of rapid technology scaling. In this talk, we present a novel technique for early prediction of timing violations in high-performance pipelined microprocessors. Through a cross layer circuit-architectural analysis, we show that a static instruction in a microprocessor, identified by its Program Counter (PC), is an excellent predictor of an upcoming timing violation. Our analysis combines architectural data collected from real program execution with gate level logic analysis. Exploiting this PC based timing violation predictability, we propose a robust system design that predicts and tolerates timing violations seamlessly in a pipelined microprocessor. Several techniques are explored for in-order and out-of-order pipelines to tolerate timing violations with minimal performance overhead.

Bio:

Dr. Sanghamitra Roy is an Assistant Professor in the department of Electrical and Computer Engineering at Utah State University. She received her Ph.D. degree in Electrical and Computer Engineering from the University of Wisconsin-Madison. She received her M.S. degree in Computer Engineering from Northwestern University in December 2003.

Dr. Roy has authored over 45 peer reviewed publications in top tier journals and conferences in CAD. She has won Best Paper Award nominations at CODES-ISSS 2014, DATE 2011, ICCAD 2005 and VLSI Design 2010. She has also won the Best Paper Award at ICCD 2012. Dr. Roy received the NSF CAREER Award in 2013. Her research is funded by the National Science Foundation (NSF), Micron Inc. and the State of Utah. Her research interests are in VLSI circuit design and optimization, and exploring reliability aware novel circuit styles and architectures.

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